LH5116S

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time: 1000 ns (MAX.)
- Low-power consumption:
  Operating: 33 mW (MAX.)
  Standby: 3.3 µW (MAX.)
- Fully-static operation
- Three-state outputs
- Single +3 V power supply
- Package: 24-pin, 450-mil SOP

DESCRIPTION

The LH5116S is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It operates at a low supply voltage of 3 V ±10%.

PIN CONNECTIONS

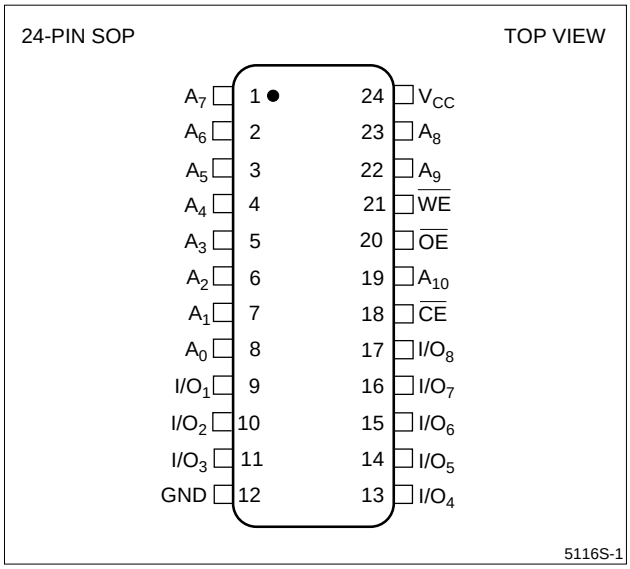


Figure 1. Pin Connections for SOP Package

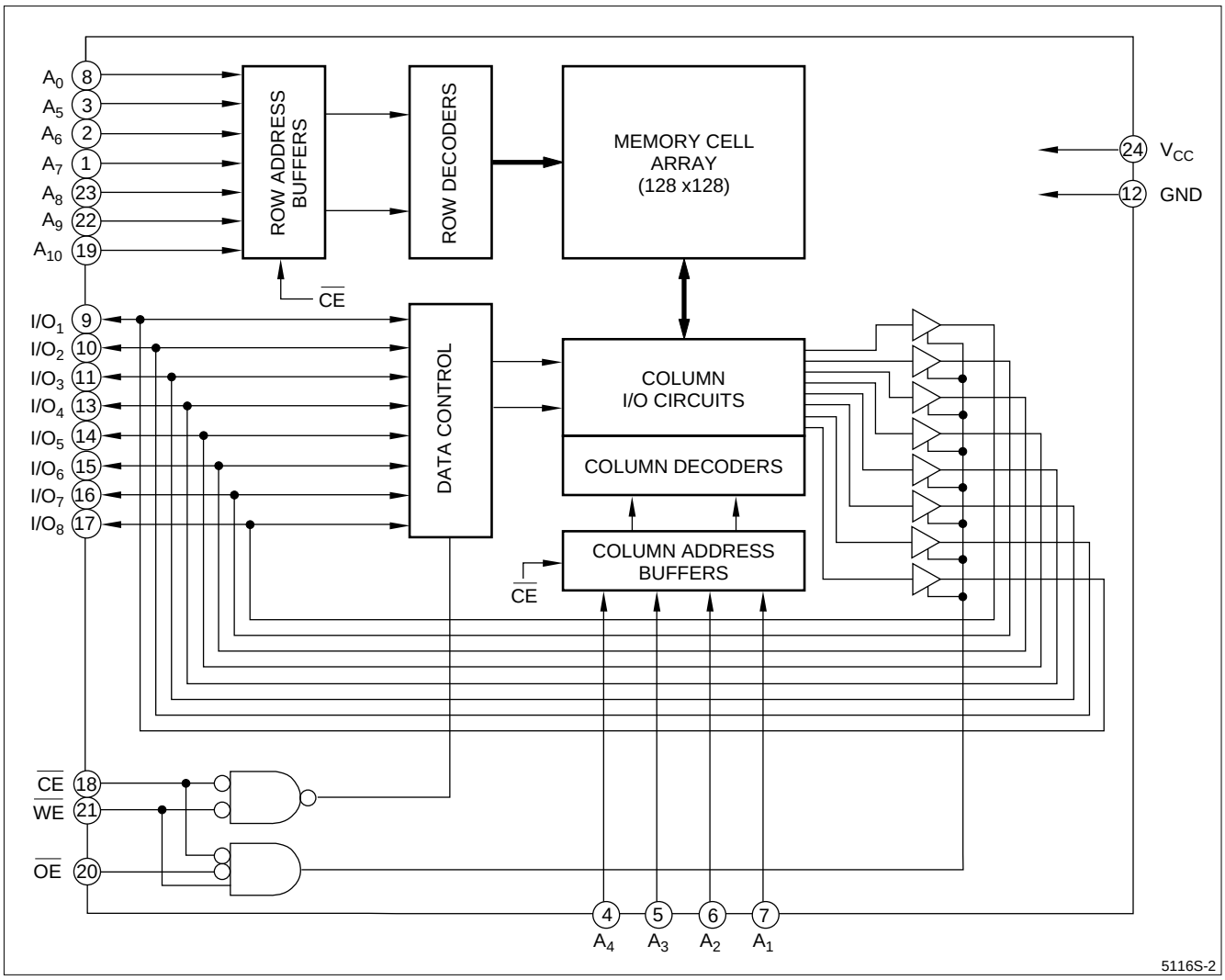


Figure 2. LH5116S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data input/output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
L	X	L	Write	D_{IN}	Operating (I_{CC})	1
L	L	H	Read	D_{OUT}	Operating (I_{CC})	
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	X	Output disable	High-Z	Operating (I_{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	0 to +50	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +50°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 3 V ±10%, T_A = 0 to +50°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output 'LOW' voltage	V_{OL}	I_{OL} = 2.1 mA			0.5	V	
Output 'HIGH' voltage	V_{OH}	I_{OH} = -1.0 mA	V_{CC} - 0.5			V	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	-1.0		1.0	µA	
Output leakage current	I_{LO}	$\overline{CE}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}	-1.0		1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{OE}$ = V_{CC})		8	10	mA	1
	I_{CC2}	Outputs open ($\overline{OE}$ = V_{IH})		8	10	mA	2
Standby current	I_{CCL}	$\overline{CE}$ ≥ V_{CC} - 0.2 V All other input pins = 0 V to V_{CC}			1.0	µA	

NOTES:
1. $\overline{CE}$ = 0 V; all other input pins = 0 V to V_{CC}
2. $\overline{CE}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}

AC CHARACTERISTICS (V_{CC} = 3 V ±10%, T_A = 0 to +50°C)

(1) READ CYCLE

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	1000			ns	
Address access time	t_{AA}			1000	ns	
Chip enable access time	t_{ACE}			1000	ns	
Chip enable Low to output in Low-Z	t_{CLZ}	10			ns	1
Output enable access time	t_{OE}			100	ns	
Output enable Low to output in Low-Z	t_{OLZ}	10			ns	1
Chip disable to output in High-Z	t_{CHZ}	0		40	ns	1
Output enable to output in High-Z	t_{OHZ}	0		40	ns	1
Output hold time	t_{OH}	10			ns	

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

(2) WRITE CYCLE (V_{CC} = 3 V ±10%, T_A = 0 to +50°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	1000			ns	
Chip enable to end of write	t_{CW}	100			ns	
Address valid time	t_{AW}	100			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	100			ns	
Write recovery time	t_{WR}	20			ns	
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	1
Data valid to end of write	t_{DW}	50			ns	
Data hold time	t_{DH}	20			ns	
Output active from end of write	t_{OW}	10			ns	1
Output enable to output in High-Z	t_{OHZ}	0		40	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

AC TEST CONDITIONS

PARAMETER	MODE	NOTE
Input voltage amplitude	0 to V_{CC}	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load conditions	C_L (100 pF)	1

NOTE:

1. Includes scope and jig capacitance.

DATA RETENTION CHARACTERISTICS (T_A = 0 to +50°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V, V_{CCDR} = 2.0 V			1.0	µA	
					0.2		1
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	2

NOTES:

1. T_A = 25°C
2. t_{RC} = Read cycle time

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:

1. This parameter is sampled and not production tested.

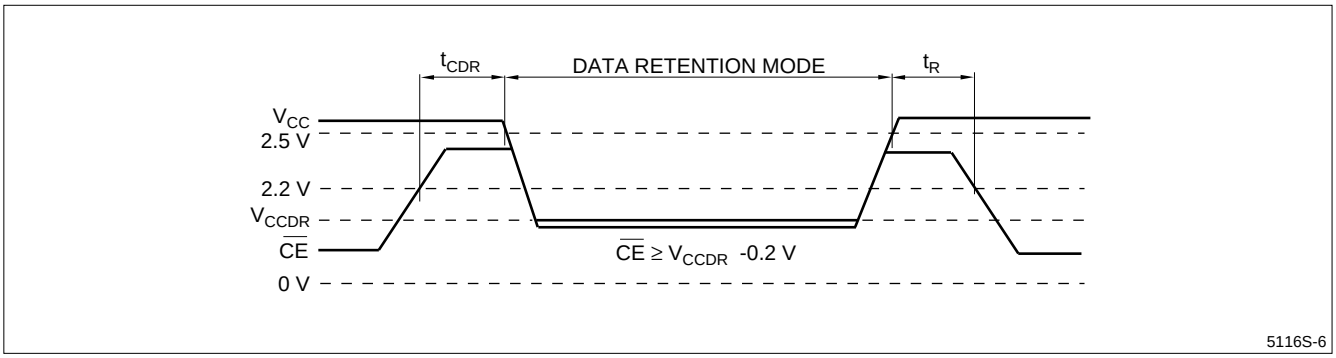


Figure 3. Low Voltage Data Retention

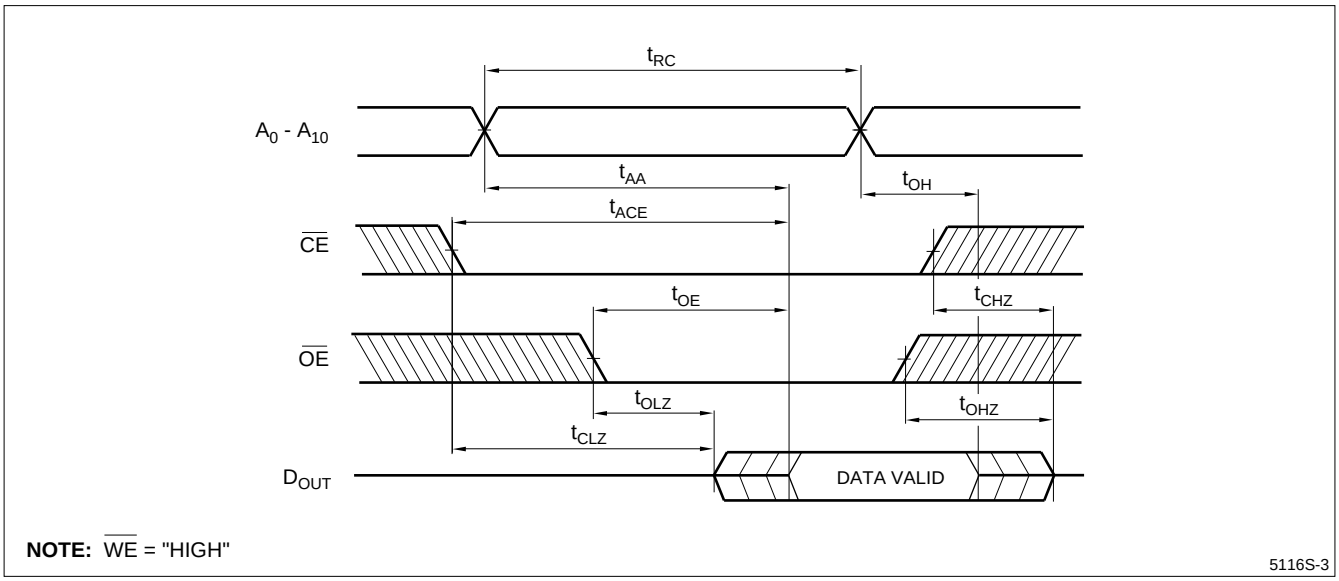
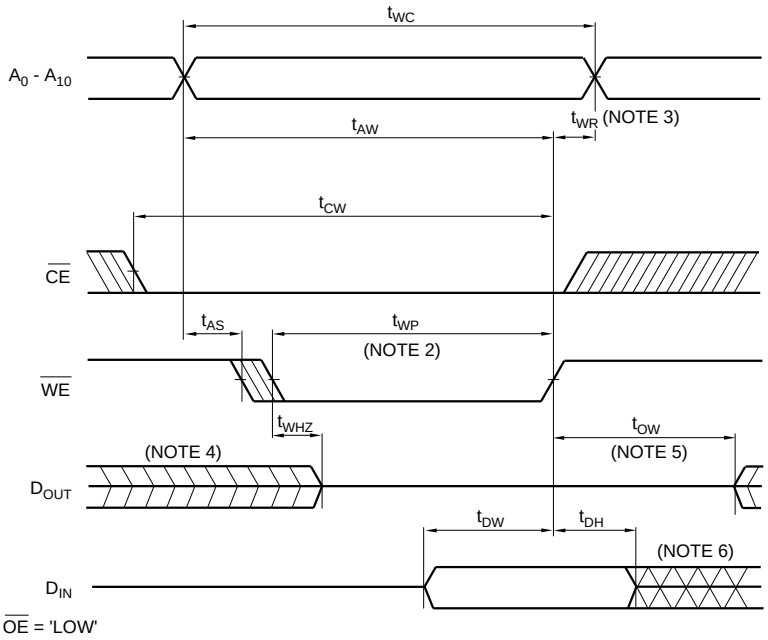


Figure 4. Read Cycle



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are both LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pins are in the output state. During this state, input signals of opposite logic level must not be applied.

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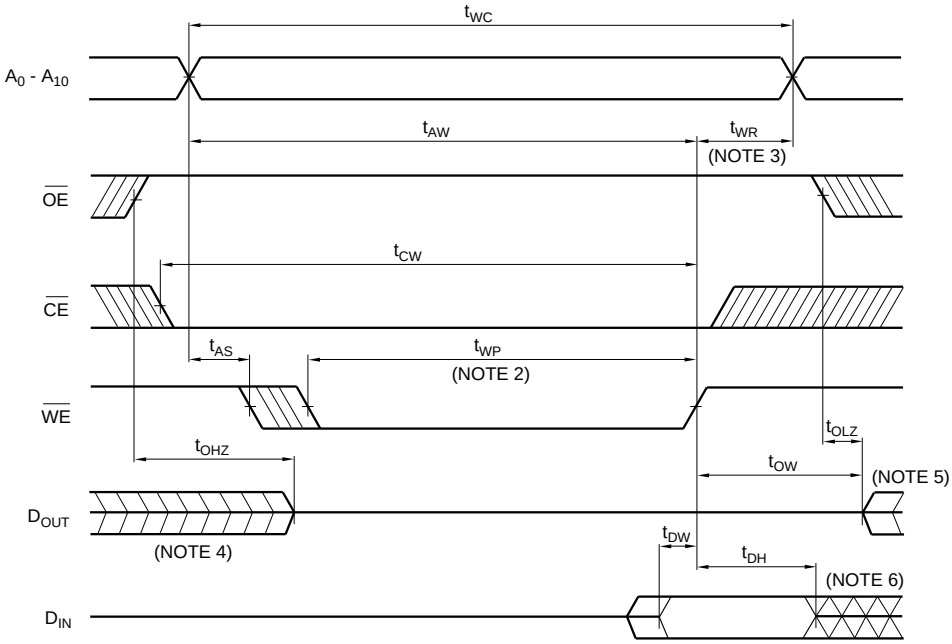
Figure 5. Write Cycle 1 (Note 1)



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are both LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ and $\overline{OE}$ are LOW during this period, the input/output pins are in the output state. During this state, input signals of opposite logic level must not be applied.

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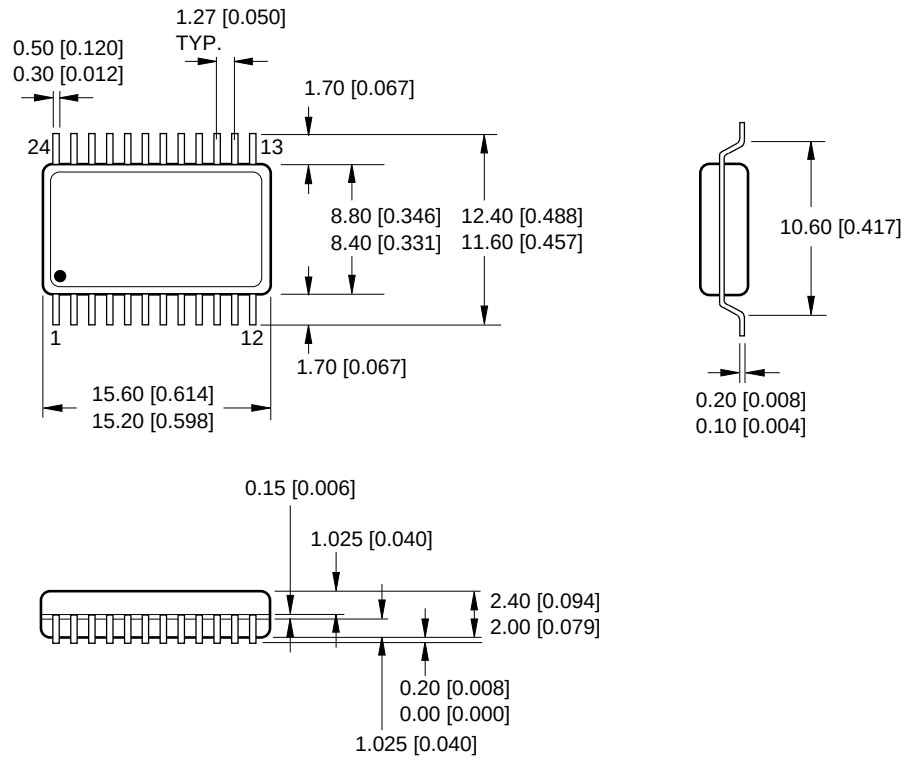
Figure 6. Write Cycle 2 (Note 1)

PACKAGE DIAGRAM

24SOP (SOP024-P-0450B)

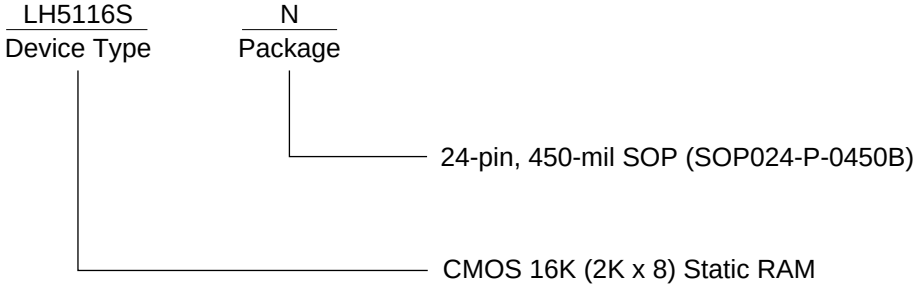


DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24SOP

24-pin, 450-mil SOP

ORDERING INFORMATION



Example: LH5116SN (CMOS 16K (2K x 8) Static RAM, 450-mil SOP)

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